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(Under Maharashtra Act No. XXIX of 2014)
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Course Structure and Detailed Syllabus

of

B. Tech Programme

for

Electronics Engineering (VLSI Design and Technology)

Third Year Engineering

In line with National Education Policy 2020

(Effective from Academic year 2026-27 for University Affiliated colleges only)

Department of Electronics Engineering
(VLSI Design and Technology)

Credit Framework under Four-Years UG Engineering Programme with Multiple Entry and Multiple Exit options:

- The Four-year Bachelor's Multidisciplinary Engineering Degree Programme allows the students to experience the full range of holistic and multidisciplinary education in addition to a focus on the chosen major and minors as per their choices and the feasibility of exploring learning from different institutions.
- The minimum and maximum credit structure for different levels under the Four-year Bachelor's Multidisciplinary Engineering UG Programme with multiple entry and multiple exit options are as given below:

Credit Framework

Levels	Qualification Title	Credit Requirements		Semester	Year
		Minimum	Maximum		
4.5	One Year UG Certificate in Engg./ Tech.	40	44	2	1
5.0	Two Years UG Diploma in Engg./ Tech.	80	88	4	2
5.5	Three Years Bachelor's Degree in Vocation (B. Voc.) or B. Sc. (Engg./ Tech.)	120	132	6	3
	4-Years Bachelor's degree				

Levels	Qualification Title	Credit Requirements		Semester	Year
		Minimum	Maximum		
6.0	(B.E./ B.Tech. or Equivalent) in Engg./ Tech. with Multidisciplinary Minor	160	176	8	4
6.0	4-Years Bachelor's degree (B.E./ B.Tech. or Equivalent) in Engg./ Tech.- Honors and Multidisciplinary Minor	180	194	8	4
6.0	4-Years Bachelor's degree (B.E./ B.Tech. or Equivalent) in Engg./ Tech.- Honors with Research and Multidisciplinary Minor	180	194	8	4
6.0	4-Years Bachelor's degree (B.E./ B.Tech. or Equivalent) in Engg./ Tech.- Major Engg. Discipline with Double Minors (Multidisciplinary and Specialization Minors)	180	194	8	4

- There are multiple exit options at each level. Student will be given a specific Qualification mentioned in the table depending on the level at which he/she decide to have an exit. Ex. If a student decides to exit after completion of two years (level 5.0) of the program, he will be given a Diploma in Engineering with specific exit condition mentioned in the syllabus of the specific branch. He/she can rejoin the program with the multiple entry option at the level next where he/she chose to exit previously. (Student can join at level 5.5 if successfully completed level 5.0 previously at the time of exit).
- Minimum credit requirements of each level are mentioned in the credit framework table.

- There are 4 distinct options available at level 6.0.
- First one is basic level 6.0 option where minimum 160-maximum 176 credits are mandatory which can be completed as per the Semester-wise Credit distribution structure mentioned in the table.

  Here, the Bachelor's Engineering Degree in chosen Engg./ Tech. Discipline with multidisciplinary minor (min.160-max.176 Credits) i.e. "**B. Tech in Electronics Engineering (VLSI Design and Technology) with Computer Engineering**" (160-176 credits) enables students to take up five-six or required additional courses of 14 credits in the discipline other than Electronics Engineering (VLSI D & T) distributed over semesters III to VIII. Here in the case of "**B. Tech in Electronics Engineering (VLSI Design and Technology) with Computer Engineering**" (160-176 credits) student is supposed to take up 50% or more courses to complete the 50% or more credits (from assigned 14 credits) from **Computer Engineering minor bucket**. The remaining courses to complete the assigned 14 credits can be covered from other discipline's minor buckets.
- Remaining three level 6.0 options are the advanced options where the student is given an opportunity to get extra qualification by earning some extra credits (18-20 extra credits). These three options are given below:
- Level 6.0: The **Bachelor's Engineering Degree with Honours** in chosen Major Engg./ Tech. Discipline i.e. in B. Tech in Electronics Engineering (VLSI Design and Technology) with Honours with Multidisciplinary Minor (180-194 credits) enables students of Electronics Engineering (VLSI Design and Technology) to take up five-six additional courses of 18 to 20 credits in the Electronics Engineering (VLSI Design and Technology) discipline distributed over semesters III to VIII. The decision regarding the mechanism of distribution of these 18-20 credits over semesters III to VIII, which are over and above the min.160-max.176 Credits prescribed for the duration of four years will be taken by Academic Authorities of University. **Student must have CGPA equal to or greater than 7.5 at the end of second semester to go for this option**.
- Level 6.0: The **Bachelor's Engineering Degree with Research** in i.e. in Electronics Engineering (VLSI Design and Technology) with Research with Multidisciplinary Minor (180-194 credits) enables students of Electronics Engineering (VLSI Design and Technology) to take up a research project of 18 to 20 credits in the Electronics Engineering (VLSI Design and Technology) discipline distributed over semesters VII to VIII. **Student must have CGPA equal to or greater than 7.5 at the end of sixth semester to go for this option**.
- Level 6.0: The **Bachelor's Engineering Degree in chosen Engg./ Tech. Discipline with Double Minor** (Multidisciplinary and Specialization Minor, 180-194 credits), i.e. "**B. Tech in Electronics Engineering (VLSI Design and Technology) with *other selected discipline in* Engineering (as MDM) with Specialization Minor in Computer Engineering**" (180-194 credits) enables students to take up five-six additional courses of 14 credits in the discipline other than Electronics Engineering (VLSI Design and Technology) (for completion of multidisciplinary minor) and 18 to 20 extra credits in the **Computer Engineering discipline** distributed over semesters III to VIII. Here, the ***other selected discipline* in Engineering should be different from Specialization Minor i.e. Computer Engineering**. This enables students to take up

five-six or required additional courses of 18 to 20 credits in the **Computer Engineering** discipline distributed over semesters III to VIII, which are over and above the min.160-max.176 Credits. The decision regarding the mechanism of distribution of these 18-20 credits over semesters III to VIII, prescribed for the duration of four years will be taken by Academic Authorities of University. **Student must have CGPA equal to or greater than 7.5 at the end of second semester to go for this option**.

Semester-wise Credit distribution structure for Four Year UG Engineering Program - One Major, One Minor

Semester		I	II	III	IV	V	VI	VII	VIII	Total Credits
Basic Science Course	BSC/ESC	06-08	08-10		--	--	--	--	--	14-18
Engineering Science Course		10-08	06-04		--	--	--	--	--	16-12
Programme Core Course (PCC)	Program Courses	--	02	08-10	08-10	10-12	08-10	04-06	04-06	44-56
Programme Elective Course (PEC)		--	--	--	--	04	08	02	06	20
Multidisciplinary Minor (MD M)	Multidisciplinary Courses		-	02	02	04	02	02	02	14
Open Elective (OE) Other than a particular program		--	--	04	02	02	--	--	--	08
Vocational and Skill Enhancement Course (VSEC)	Skill Courses	02	02	--	02	--	02	--	--	08
Ability Enhancement Course (AEC -01, AEC-02)	Humanities Social Science and Management (HSSM)	02	--	--	02	--	--	--	--	04
Entrepreneurship/Economics/ Management Courses		--		02	02	--	--	--	--	04
Indian Knowledge System (IKS)			02		--	--	--	--	--	02
Value Education Course (VEC)		--	--	02	02	--	--	--	--	04
Research Methodology	Experiential Learning Courses	--	--	--	--	--	--		04	04
Comm. Engg. Project (CEP)/Field Project (FP)		--	--	02	--	--	--	-	-	02
Project		--	--	--	--	--	--		04	04
Internship/ OJT		--	---			--	--	12	-	12
Co-curricular Courses (CC)	Liberal Learning Courses	02	02		--	--	--	--	-	04
Total Credits (Major)		**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**160-176**

Student need to follow the Semester-wise Credit distribution structure for Four Year UG Engineering Program as prescribed in the table given above.

- There are seven vertical categories with specific credits distributed in specific semesters.
- Student can choose a Program Elective Course (PEC) in that specific semester from the given subjects.
- Multidisciplinary course (MDM) and Open Elective (OE) courses can be chosen from the MDM and OE Buckets depending on students' choice. Completion of total credits given in the last column of the table for each vertical is mandatory.
- Students can complete 40% of the courses through online platforms like NPTEL/SWAYAM. The NPTEL SWAYAM course content should be at least 80% similar to the course content in the syllabus.

General Rules and Regulations

1. The normal duration of the course leading to B.Tech degree will be EIGHT semesters.

2. The normal duration of the course leading to M.Tech. degree will be FOUR semesters.

3. Each academic year shall be divided into 2 semesters, each of 20 weeks duration, including evaluation and grade finalization, etc. The Academic Session in each semester shall provide for at least 90 Teaching Days, with at least 40 hours of teaching contact periods in a five to six days session per week. The semester that is typically from Mid-July to November is called the ODD SEMESTER, and the one that is from January to Mid-May is called the EVEN SEMESTER. Academic Session may be scheduled for the Summer Session/Semester as well. For 1st year B. Tech and M. Tech the schedule will be decided as per the admission schedule declared by Government of Maharashtra.

4. The schedule of academic activities for a Semester, including the dates of registration, mid-semester examination, end-semester examination, inter-semester vacation, etc. shall be referred to as the Academic Calendar of the Semester, which shall be prepared by the Dean (Academic), and announced at least TWO weeks before the Closing Date of the previous Semester.

5. The Academic Calendar must be strictly adhered to, and all other activities including cocurricular and/or extra -curricular activities must be scheduled so as not to interfere with the Curricular Activities as stipulated in the Academic Calendar.

Registration:

1. Lower and Upper Limits for Course Credits Registered in a Semester, by a Full- Time Student of a UG/PG Programme:

   A full time student of a particular UG/PG programme shall register for the appropriate number of course credits in each semester/session that is within the minimum and maximum limits specific to that UG/PG programme as stipulated in the specific Regulations pertaining to that UG/PG programme.
2. Mandatory Pre-Registration for higher semesters: In order to facilitate proper planning of the academic activities of a semester, it is essential for the every institute to inform

to Dean (Academics) and COE regarding details of total no. of electives offered (Course-wise) along with the number of students opted for the same. This information should be submitted within two weeks from the date of commencement of the semester as per academic calendar.

3. PhD students can register for any of PG/PhD courses and the corresponding rules of evaluation will apply.
4. Under Graduate students may be permitted to register for a few selected Post Graduate courses, in exceptionally rare circumstances, only if the DUGC/DPGC is convinced of the level of the academic achievement and the potential in a student.

Course Pre-Requisites:

1. In order to register for some courses, it may be required either to have exposure in, or to have completed satisfactorily, or to have prior earned credits in, some specified courses.
2. Students who do not register on the day announced for the purpose may be permitted LATE REGISTRATION up to the notified day in academic calendar on payment of late fee.
3. REGISTRATION IN ABSENTIA will be allowed only in exceptional cases with the approval of the Dean (Academic) / Principal.
4. A student will be permitted to register in the next semester only if he fulfils the following conditions:

   i) Satisfied all the Academic Requirements to continue with the programme of Studies without termination ii) Cleared all Institute, Hostel and Library dues and fines (if any) of the previous semesters;

   iii) Paid all required advance payments of the Institute and hostel for the current semester;

   iv) Not been debarred from registering on any specific ground by the Institute.

Evaluation System:

1. Absolute grading system based on absolute marks as indicated below will be implemented from academic year 2024-25, from I year B. Tech.

Percentage of marks	Letter Grade	Grade Point
91-100	EX	10.0
86-90	AA	9.0
81-85	AB	8.5
76-80	BB	8.0
71-75	BC	7.5

66-70	CC	7.0
61-65	CD	6.5
56-60	DD	6.0
51-55	DE	5.5
40-50	EE	5.0
<40	EF	0.0

2. Class is awarded based on CGPA of all eighth semester of B. Tech Program.

CGPA for pass is minimum 5.0	
CGPA up to <5.50	Pass class
CGPA ≥ 5.50&<6.00	Second Class
CGPA ≥ 6.00&<7.5	First Class
CGPA >7.50	Distinction
[Percentage of Marks =CGPA*10.0]	

3. A total of 100 Marks for each theory course are distributed as follows:

Mid Semester Exam (MSE) Marks	20
Continuous Assessment Marks	20
End Semester Examination (ESE)Marks	60

4. A total of 100 Marks for each practical course are distributed as follows

1.	Continuous Assessment Marks	40
2.	End Semester Examination (ESE)Marks	60

- It is mandatory for every student of B. Tech to score a minimum of 40 marks out of 100, M. Tech to score a minimum of 45 marks out of 100 with a minimum of 20 marks out of 60 marks in End Semester Examination for theory course.
- This will be implemented from the first year of B. Tech starting from Academic Year 2024-25

5. Description of Grades

EX Grade: An "EX" grade stands for outstanding achievement.

EE Grade: The "EE" grade stands for minimum passing grade.

If any of the students remain absent for the regular examination due to genuine reason and the same will be verified and tested by the Dean (Academics) or committee constituted by the University Authority.

FF Grade: The "FF" grade denotes very poor performance, i.e. failure in a course due to poor performance. The students who have been awarded "FF" grade in a course in any semester must repeat the subject in next semester.

6. Evaluation of Performance

a. Semester Grade Point Average (SGPA)

The performance of a student in a semester is indicated by Semester Grade Point Average (SGPA) which is a weighted average of the grade points obtained in all the courses taken by the student in the semester and scaled to a maximum of 10. (SGPI is to be calculated up to two decimal places). A Semester Grade Point Average (SGPA) will be computed for each semester as follows:

$$SGPA = \frac{[\sum_{i=1}^{n} c_i g_i]}{[\sum_{i=1}^{n} c_i]}$$

Where

"n" is the number of subjects for the semester,

"c_i" is the number of credits allotted to a particular subject, and

"g_i" is the grade-points awarded to the student for the subject based on his performance as per the above table.

SGPA will be rounded off to the second place of decimal and recorded as such.

b. Cumulative Grade Point Average (CGPA):

An up to date assessment of the overall performance of a student from the time he entered the Institute is obtained by calculating Cumulative Grade Point Average (CGPA) of a student. The CGPA is weighted average of the grade points obtained in all the courses registered by the student since s/he entered the Institute. CGPA is also calculated at the end of every semester (up to two decimal places). Starting from the first semester at the end of each semester (S), a Cumulative Grade Point Average (CGPA) will be computed as follows:

$$CGPA = \frac{[\sum_{i=1}^{m} c_i g_i]}{[\sum_{i=1}^{m} c_i]}$$

Where,

"m" is the total number of subjects from the first semester onwards up to and including the semester S,

"ci" is the number of credits allotted to a particular subject, and

"gi" is the grade-points awarded to the student for the subject based on his/her performance as per the above table.

CGPA will be rounded off to the second place of decimal and recorded as such.

7. Attendance Requirements:

a. All students must attend every lecture, tutorial and practical classes.

b. To account for approved leave of absence (eg. representing the Institute in sports, games or athletics; placement activities; NCC/NSS activities; etc.) and/or any other such contingencies like medical emergencies, etc., the attendance requirement shall be a minimum of 75% of the classes actually conducted. If the student failed to maintain 75% attendance, he/she will be detained for appearing the successive examination. The Dean (Academics)/ Principal is permitted to give 10% concession for the genuine reasons as such the case may be. In any case the student will not be permitted for appearing the examination if the attendance is less than 65%.

c. The course instructor handling a course must finalize the attendance 3 calendar days before the last day of classes in the current semester and communicate clearly to the students by displaying prominently in the department and also in report writing to the head of the department concerned.

d. The attendance records are to be maintained by the course instructor and he shall show it to the student, if and when required.

8. Transfer of Credits:

The courses credited elsewhere, in Indian or foreign University/Institutions/ Colleges/Swayam Courses by students during their study period at DBATU may count towards the credit requirements for the award of degree. The guidelines for such transfer of credits are as follows:

a. 20 % of the total credit will be considered for respective calculations.

b. Credits transferred will be considered for overall credits requirements of the programme.

c. Credits transfer can be considered only for the course at same level i.e UG, PG etc.

d. A student must provide all details (original or attested authentic copies) such as course contents, number of contact hours, course instructor /project guide and evaluation system for the course for which he is requesting a credits transfer. He shall also provide the approval or acceptance letter from the other side. These details will be evaluated by the concerned Board of Studies before giving approval. The Board of Studies will then decide the number of equivalent credits the student will get for such course(s) in DBATU. The complete details will then be forwarded to Dean for approval.

e. A student has to get minimum passing grades/ marks for such courses for which the credits transfers are to be made.

f. Credits transfers availed by a student shall be properly recorded on academic record(s) of the student.

g. In exceptional cases, the students may opt for higher credits than the prescribed.

THIRD YEAR SYLLABUS STRUCTURE FOR
ELECTRONICS ENGINEERING (VLSI DESIGN AND TECHNOLOGY)

Semester V											
Sr. No.	**Course Category**	**Course Code**	**Course Title**	**Teaching Scheme**			**Evaluation Scheme**				**Credit**
				L	**T**	**P**	**CA**	**MSE**	**ESE**	**Total**	
1	PCC	26AF1378PC501	CMOS VLSI Design	3	0	0	20	20	60	100	3
2	PCC Lab	26AF1378PC502L	CMOS VLSI Design Lab	0	0	2	60	--	40	100	1
3	PCC	26AF1378PC503	Microcontroller & Its Applications	3	0	0	20	20	60	100	3
4	PCC Lab	26AF1378PC504L	Microcontroller & its Applications Lab	0	0	2	60	--	40	100	1
5	OE	26AF1XXXOE505	**Open Elective Bucket****	3	0	0	20	20	60	100	3
6	MD Minor	26AF1378MD506	**MDM Bucket***	2	0	0	20	20	60	100	2
7	PCC	26AF1378PC507	Digital Signal and Image Processing	3	0	0	20	20	60	100	3
8	PCC Lab	26AF1378PC508L	Digital Signal and Image Processing Lab	0	0	2	60	--	40	100	1
9	PEC	26AF1378PE509A	Control System Engineering	3	1	0	20	20	60	100	4
		26AF1378PE509B	Power Electronics								
		26AF1378PE509C	Information Theory & Coding Techniques								
			Total	**17**	**1**	**6**				**900**	**21**

NOTE: *Refer to Multidisciplinary Minor Bucket
****Refer to Open Elective Bucket**

THIRD YEAR SYLLABUS STRUCTURE FOR ELECTRONICS ENGINEERING (VLSI DESIGN AND TECHNOLOGY)

Semester VI											
Sr. No.	**Course Category**	**Course Code**	**Course Title**	**Teaching Scheme**			**Evaluation Scheme**				**Credit**
				L	**T**	**P**	**CA**	**MSE**	**ESE**	**Total**	
1	PCC	26AF1378PC601	SystemVerilog for Design and Verification	3	0	0	20	20	60	100	3
2	PCC Lab	26AF1378PC602L	SystemVerilog for Design and Verification Lab	0	0	2	60	--	40	100	1
3	PCC	26AF1378PC603	Embedded System Design	3	0	0	20	20	60	100	3
4	PCC Lab	26AF1378PC604L	Embedded System Design Lab	0	0	2	60	--	40	100	1
5	PEC	26AF1378PE605A	Introduction to VLSI Life Cycle & Microfabrication	3	1	0	20	20	60	100	4
		26AF1378PE605B	Digital VLSI Design								
		26AF1378PE605C	Computer Networks								
6	MD Minor	26AF1378MD606	**MDM Bucket***	3	0	0	20	20	60	100	3
7	PEC	26AF1378PE607A	IC Packaging	3	1	0	20	20	60	100	4
		26AF1378PE607B	Electromagnetic Field Theory								
		26AF1378PE607C	Advanced Communication Technology								
8	VSEC	26AF1378SE608	Basic Concepts of Film & Video Editing	1	0	2	60	--	40	100	2
			Total	**16**	**2**	**6**				**800**	**21**

NOTE: *Refer to Multidisciplinary Minor Bucket

Credit Distribution

SEM I	SEM II	SEM III	SEM IV	SEM V	SEM VI	SEM VII	SEM VIII	TOTAL
23	21	23	24	21	21	24	19	176

For Degree completion: Students must complete min 08 Credits of Open Elective, 20 Credits of Program Elective, 14 Credits of HSSM, 4 credits of co-curricular courses and 22 credits of Experiential learning courses from Open courses slots Institutes are free to manage the slots according to BoS inputs.

NOTE: Students can complete 40% of the courses through online platforms like NPTEL/SWAYAM. The NPTEL SWAYAM course content should be at least 80% similar to the course content in the syllabus.

BSC / ESC	Program Courses (PCC & PEC)	Multidisciplinary Courses (MDM)	Multidisciplinary Courses (OE)	Skill Courses (VSEC)	Humanities Social Science & Management (HSSM) (IKS, VEC, AEC)	Experiential Learning Courses (CEP & FP)	Liberal Learning Courses (CC)	TOTAL
34	70	14	8	8	16	22	4	176

Multidisciplinary Minor Domains

Label	Multi-Disciplinary Minor Domains	SY		TY		B-Tech		Offered to students of B Tech Program
		MD1-1	MD2-2	MD3-3	MD4-4	MD5-5	MD5-6	
		Sem-III	Sem-IV	Sem-V	Sem-VI	Sem-VII	Sem-VIII	
MD1	VLSI Design & Technology	Digital System Design & Microprocessor	System Design using Verilog	CMOS VLSI Design	SystemVerilog for Design and Verification	A. Analog VLSI Design B. FPGA Architecture & VHDL Programming	Capstone Project	ALL (Except EE (VLSI D & T) Students)

Open Electives

In the vertical of Multidisciplinary courses, students need to cover Open Elective Courses (OE) of 08 credits. These 08 credits over semesters III to V, which are included in the basic min.160-max.176 Credits. It is offered in Second and/or Third year. Refer to Semester wise credit distribution table given below. Faculty-wise baskets of OE are prepared by university which are chosen from faculty other than that of the Major Faculty i.e. in this case Major Faculty is Faculty of Engineering.

Other Faculties considered are as follows:

1. Faculty of Management and Commerce
2. Faculty of Law
3. Faculty of Humanities and Arts
4. Faculty of Architecture and Planning
5. Faculty of Health Sciences
6. Faculty of Science

Students need to take up three-four courses of 08 credits over semesters III to V.

Third Year (Semester V)
CMOS VLSI Design

26AF1378PC501	CMOS VLSI Design	PCC	3L- 0T - 0P	3 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 0 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. Explain the operational physics, small-geometry effects, and fabrication layout rules of MOS transistors.
2. Illustrate the static voltage transfer characteristics and transient delay metrics of the complementary CMOS inverter.
3. Apply complementary CMOS, pass-transistor, and transmission gate architectures to realize complex Boolean logic.
4. Calculate the optimized delay paths in standard logic networks utilizing logical effort methodologies.
5. Examine the signal degradation effects caused by resistive, capacitive, and inductive interconnect parasitics.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the VLSI Design flow, current-voltage parameters and device physics of MOSFET devices.
CO2	Compare the noise margins, threshold voltages, and power dissipation metrics of CMOS inverters.
CO3	Construct optimized combinational logic circuits using standard Ratioless and transmission gate styles.
CO4	Apply power & delay optimization techniques for CMOS logic
CO5	Design CMOS logic layouts and stick diagrams adhering to standard fabrication technologies.

UNIT-I MOS TRANSISTOR BASICS **[08 Hours]**

Overview: VLSI Design Flow: Full custom and Semicustom IC design flow.

Device Physics: The MOS Structure, MOSFET Current-Voltage characteristics, threshold voltage, body effect. Operational regions, MOSFET capacitances. Small-Geometry Effects, Small Signal Model.

UNIT II: MOSFET Inverters **[08 Hours]**

Introduction to MOS inverters: Active and passive load nMOS inverters, NMOS inferior pull up device, PMOS inferior pull up device.

Static Characteristics of CMOS Inverter: CMOS Inverter, Voltage Transfer Characteristics (VTC), Inverter threshold voltage, Calculation of Critical Voltages, noise margins.

Transient & Power Analysis of CMOS Inverter: Rise time, fall time, delay estimations. Power Dissipation (dynamic, static, short-circuit), latch up.

UNIT III: BASIC COMBINATIONAL LOGIC DESIGN **[08 hours]**

Combinational CMOS Design: Primitive logic gates (NOR & NAND) & realizing complex Boolean expressions using CMOS logic, AOI and OAI gates, CMOS Full Adder Circuit.

Pass-Transistor & Transmission Gate Logic: Pass Transistor logic, CMOS Transmission Gate logic, Basic gates and MUX realization using pass transistor and transmission gate logic.

UNIT IV: Power & Delay Economy & Logical Efforts in CMOS logic [08 Hours]

Power & Delay Economy: Ways to reduce power in CMOS logic**,** Estimation of Interconnect resistance, Estimation of interconnect capacitance, RC delay model: lumped model, Ways for Reduction of RC delay, Introduction to BiCMOS logic.

Logical Efforts: Basics of logical efforts, calculation of logical efforts for logic gates, electrical effort, and optimizing delay in multistage networks.

UNIT V: CMOS Fabrication & Layout Design Rules [08 Hours]

CMOS Fabrication Flow: CMOS fabrication process flow & technologies.

CMOS Design Layout: Layout Design Rules: Lambda and Micron rules, Stick Diagram, Optimization of Stick Diagram using Euler Graph, Stick Diagram for simple and complex CMOS logic circuits.

Technology Related CAD Issues: Design Rule Checking, Layout Versus Schematic Check.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici "CMOS Digital Integrated Circuits Analysis and Design", TMH, 3rd Ed., 2011.
2. John P. Uyemura, "CMOS LOGIC CIRCUIT DESIGN", KLUWER ACADEMIC PUBLISHERS, 2002
3. Ken Martin, "Digital Integrated Circuit Design", Oxford Press, 2000.
4. Neil H.E. Weste and Harris, "CMOS VLSI Design: A Circuits and Systems Perspective".

REFERENCES:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd Ed., PHI.
2. Neil H.E. weste and Kamran Eshraghian, "Principles of CMOS vlsi design: A system Perspective".
3. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press, 2011
4. John Wakerly, "Digital Design – Principles and Practices", Pearson.

Third Year (Semester V)
CMOS VLSI Design Lab

26AF1378PC502L	CMOS VLSI Design Lab	PCC Lab	0L- 0T - 2P	1 Credits

Teaching Scheme	Examination Scheme
Practical: 02 hrs./week	Continuous Assessment: 60 Marks End Semester Exam: 40 Marks

CMOS VLSI Design Lab

(Minimum 8-10 experiments are to be performed based on contents from syllabus)

Sample List of Practical's:

1. CMOS Inverter Static and Transient Analysis.
2. Physical Layout and DRC of a CMOS Inverter.
3. Physical Layout & DRC of a 3 input NAND or NOR Gate in CMOS logic.
4. Physical Layout & DRC of a 2 input XOR Gate in CMOS logic.
5. Optimization of layout using Euler Paths for Complex logic circuit in CMOS logic.
6. Practical to demonstrate the difference between automated and manual layout in layout design software. Automated Layout generated from the HDL file.
7. Design & implement One-bit full adder in sub-micron CMOS technology.
8. Practical based on BiCMOS logic
9. Practical based on Pass-Transistor Logic
10. Practical based on Transmission Gate logic
11. Design a CMOS Full Adder and verify functionality.
12. Practical to demonstrate Layout versus Schematic.
13. Design a Transmission Gate-based 2:1 multiplexer and verify logic operation.
14. Mini project.

Third Year (Semester V)
Microcontroller & Its Applications

26AF1378PC503	Microcontroller & Its Applications	PCC	3L- 0T - 0P	3 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 0 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

The aim of this course is to:

1. Understand the architecture and features of microcontrollers and embedded systems.
2. Demonstrate the operation of memory organization, instruction set, timers, interrupts, and serial communication of 8051 microcontroller.
3. Interface peripheral devices and sensors with 8051.
4. Design basic embedded system applications using microcontrollers.
5. Understand the different families of ARM processor.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Explain the fundamentals of microcontrollers, processor architectures, and features of 8051 microcontroller.
CO2	Demonstrate the operation of memory organization, instruction set, timers, interrupts, and serial communication of 8051 microcontroller.
CO3	Interface input/output devices, displays, sensors, and actuators with 8051 microcontroller using Embedded C.
CO4	Build basic embedded system applications such as waveform generation, motor control, soil monitoring, and home automation systems using microcontrollers.
CO5	Describe the programmer's model of the ARM processor.

Course Contents:

Unit 1: Introduction to Microcontrollers [08 Hours]

Microprocessors v/s Micro-controllers, Types of Micro-controllers, Selection of Microcontroller, External Memory, Processor Architecture – Harvard v/s Von Neumann; CISC v/s RISC, Software Tools: Assembler, Compiler, IDE, Debugger, Programmer.

Unit 2: 8051 Microcontroller [08 Hours]

8051 Microcontroller: Features & Pin configuration, Block Diagram of 8051. Port Structure, Memory Organization, Interrupt handling, Timers of 8051, Serial Communication, addressing modes, Instruction Set of 8051, Assembly language programming (ALP): Addition, Multiplication, Substraction, Division code.

Unit 3: Interfacing & Programming of 8051 [08 Hours]

Difference between 'C' and Embedded C, Programming of 8051 using embedded C language.

Interfacing: LEDs, Push Buttons, Relays, Keyboard, Seven Segment and LCD display interfacing, I2C bus operation, DC Motor interfacing using motor driver (All Programs in embedded C language).

Unit 4: Microcontroller Applications [08 Hours]

Square and Triangular waveform generation using DAC, Temperature sensor interfacing using ADC, Water Level controller using 8051, Stepper Motor Interfacing to 8051, Soil Monitoring System for agriculture, Home Automation System.

Unit 5: ARM Microcontroller Architecture [08 Hours]

Introduction to ARM processors and its versions, ARM7, ARM9 & ARM11 features and comparison, registers, CPSR, SPSR, ARM and RISC design philosophy, ARM7 data flow model, programmers model, modes of operations, ARM 3 stage Pipeline, ARM 5 stage Pipeline.

Text Books

1. Mazidi, M. A., Mazidi, J. G., & McKinlay, R.D. (2006). The 8051 microcontroller and embedded systems: using Assembly and C, Pearson/Prentice Hall.
2. Kenneth J. Ayala, Dhananjay V. Gadre, "The 8051 Microcontroller & Embedded Systems Using Assembly and C", Cengage Learning India Publication.
3. Andrew Sloss, Dominic Symes, Chris Wright, ARM System Developer's Guide Designing and Optimizing System Software‖, ELSEVIER.

Reference Books

1. Microcontrollers Architecture Programming Interfacing and System Design, Raj Kamal, Pearson Education.
2. The 8051 Microcontroller Based Embedded Systems, Manish K. Patel, McGraw Hill Education.
3. The 8051 Microcontroller A Systems Approach, Muhammad Ali Mazidi, Janice Gillispie Mazidi, R. D. McKinlay.
4. Raj Kamal, "Embedded Systems", TMH.
5. Shibu K," Embedded Systems", Tata McGraw Hill Publishing.
6. ARM architecture reference manual: - www.arm.com
7. RENESAS Microcontroller:- www.renesas.com

Third Year (Semester V)
Microcontroller & Its Applications Lab

26AF1378PC504L	Microcontroller & Its Applications Lab	PCC Lab	0L- 0T - 2P	1 Credits

Teaching Scheme	Examination Scheme
Practical: 02 hrs./week	Continuous Assessment: 60 Marks End Semester Exam: 40 Marks

Microcontroller & Its Applications Lab

(Minimum 8-10 experiments are to be performed based on contents from syllabus)

Sample List of Practical's:

1. Study and Identification of Various Pins, Blocks, and Interfaces of 8051 Microcontroller Development Board.
2. Develop and Execute Assembly Language or Embedded C Programs using an Integrated Development Environment (Keil/MicroPro).
3. Interface LED with 8051 Microcontroller and Turn it ON using External Interrupt.
4. Interface 7-Segment Display with 8051 Microcontroller and Display Numbers from 0 to 9 with Specific Delay (Embedded C).
5. Interface 16×2 LCD Display with 8051 Microcontroller and Display a String using Embedded C.
6. Interface 4×4 Keypad and 16×2 LCD Display with 8051 Microcontroller and Display Pressed Key Value on LCD.
7. Interface Relay with 8051 Microcontroller and Control ON/OFF Operation using Embedded C.
8. Interface Stepper Motor with 8051 Microcontroller and Control its Clockwise and Counterclockwise Rotation at Different Speeds.
9. Interface 8-bit ADC/ DAC with 8051 Microcontroller and Write a C Program to Convert Analog Signal to Digital and Store the Data in Memory or Generate Square and Sawtooth Waveforms using Embedded C.
10. Case Study on Classification and Application of Embedded Systems.
11. Mini Project: Design and Demonstrate a Simple Embedded Application using 8051 Microcontroller (e.g., Temperature Display, Automatic Light Control, or Motor Speed Control)

Third Year (Semester V)
Digital Signal and Image Processing

26AF1378PC507	Digital Signal and Image Processing	PCC	3L- 0T - 0P	3 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 0 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. Introduce fundamental concepts of discrete-time signals and digital signal processing.
2. Develop understanding of Z-transform and its application in system analysis.
3. Explain frequency domain representation using DFT and FFT techniques.
4. Understand basic of Digital image processing and Image Enhancement techniques.
5. Explore Image Morphological Operations and Segmentation Techniques.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Explain discrete-time signals, sampling concepts, and basic principles of digital signal processing.
CO2	Apply Z-transform techniques to analyze systems and solve difference equations.
CO3	Convert signals in frequency domain using DFT and FFT algorithms.
CO4	Understand basic of Digital image processing and Image Enhancement techniques.
CO5	Apply Image Morphological Operations and Segmentation Techniques.

Course Contents:

Unit 01: Fundamental of DSP **[8 hours]**

Sampling and reconstruction of signals, Discrete time signals, representation of DT signals, operations on DT Signals, Basic elements of DSP, advantages of DSP over ASP, Classification of Discrete Time Signals, Classification of Discrete Time Systems, LTI Systems, Convolution.

Unit 2: Z transform **[7 hours]**

Need for transform, Definition & Properties of Z-Transform, ROC & its properties, System Stability in Z-domain, Inverse Z transform: Power series method, Partial Fraction Expansion method, Solution of difference equations.

Unit 3: Discrete Fourier Transform **[8 Hours]**

DTFT: Definition & Properties, Frequency domain sampling.
DFT: Properties, circular convolution, Computation of linear convolution using DFT, IDFT
FFT: Decimation in time and Decimation in frequency using Radix-2 FFT algorithm.

Unit 4: Introduction to DIP & Image Enhancement **[10Hours]**

Motivation & Perspective, Applications, Types of images, Fundamentals Steps in Image Processing, Components of Image Processing System, Image digitization, Some basic relationships, Distance Measures between pixels, Image basic operation, Special Operations.

Image Enhancement: Introduction, Basic Intensity Transformation: Image Negatives, Log transformation, Power law Transformation, piecewise linear transformation functions, Histogram processing, Histogram Equalization and Matching.
Basics of Spatial Filters, Smoothening (LPF) (Linear: Box, Gaussian & Non Linear: Median) and Sharpening (HPF): Laplacian operators.

Unit 5: Morphological operations and segmentation [07 Hours]
Introduction, erosion, dilation, opening, closing, Hit or Miss, boundary extraction, thinning, thickening.
Segmentation: Fundamentals; Point, Line and Edge Detection; Basics of edge detection: Image gradient and operators, Thresholding: Intensity Thresholding, Global thresholding, Segmentation by region growing, region splitting and merging.

Text Books:

1. Dr. S. L. Nalbalwar, A.M. Kulkarni and S.P. Sheth, "Signals and Systems", 2nd Edition, Synergy Knowledgeware,2017.
2. Nagoor Kanni "Digital Signal Processing", 2nd edition, McGrawHill.
3. R. C. Gonzalez, R. E. Woods, Digital Image Processing. Addison Wesley Longman, Inc.,4th Edition, 2018.

Reference Books:

1. Alan V. Oppenheim. Alan S. Willsky and S. Hamid Nawab, "Signals and Systems",PHI
2. A.V. Oppenheim and Schafer, Discrete Time Signal Processing, Prentice Hall, 1989.
3. John G. Proakis and D.G. Manolakis, Digital Signal Processing: Principles, Algorithms And Applications, Prentice Hall, 1997.
4. D. H. Ballard, C. M. Brown. Computer Vision. Prentice-Hall, Englewood Cliffs, 1982.
5. Richard Szeliski, Computer Vision: Algorithms and Applications (CVAA). Springer, 2010
6. Image Processing, Analysis, and Machine Vision. Sonka, Hlavac, and Boyle. Thomson.

Third Year (Semester V)
Digital Signal and Image Processing Lab

26AF1378PC508L	**Digital Signal and Image Processing Lab**	**PCC Lab**	**0L- 0T - 2P**	**1 Credits**

Teaching Scheme	Examination Scheme
Practical: 02 hrs./week	Continuous Assessment: 60 Marks End Semester Exam: 40 Marks

Digital Signal and Image Processing Lab

Minimum 8-10 experiments are to be performed based on contents from syllabus.

Third Year (Semester V)
A. Control System Engineering

26AF1378PE509A	Control System Engineering	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

The aim of this course is to:

1. To Introduce elements of control systems and their modelling using various Techniques.
2. To get acquainted with the methods for analysing the time response (Time Domain Analysis).
3. To Introduce and analyse the stability of the System.
4. To Introduce the concept of Bode plots, Nyquist plots with the help of frequency Domain Analysis.
5. To apply the concepts of state-space representation.

Course Outcomes:

On completion of the course, students will be able to:

CO1	To identify basic components of control systems and develop mathematical models using block diagrams and transfer functions.
CO2	To analyze the time response of systems and evaluate performance.
CO3	To determine system stability using Routh-Hurwitz and Root Locus techniques and assess the impact of pole locations on stability.
CO4	To construct and interpret Bode and Nyquist plots for control systems stability in the frequency domain.
CO5	To formulate state-space models of LTI systems using various methods.

Course Contents:

Unit I: Introduction to Control Systems & its modelling [08 Hours]

Basic Elements of Control System, Open loop and Closed loop systems, Differential equations and Transfer function, Modelling of Electric systems, Translational and rotational mechanical systems, Block diagram reduction Techniques, Signal flow graph.

Unit II: Time domain analysis [08 Hours]

Time domain analysis: transient response and steady state response, standard test inputs for time domain analysis, order and type of a system, transient analysis of first and second order systems, time domain specifications of second order under-damped system from its step response, steady state error and static error constants.

Unit III: Stability analysis [08 Hours]

Characteristic equation of a system, concept of pole and zero, response of various pole locations in s plane, concept of stability, absolute stability, relative stability, stability of system from pole locations, Routh Hurwitz stability criterion, Root locus: definition, magnitude and angle conditions, construction of root locus, concept of dominant poles, effect of addition of pole and zero on root locus.

Unit IV: Frequency domain analysis [08 Hours]

Frequency response and frequency domain specifications, correlation between time domain and frequency domain specifications, polar plot, Nyquist stability criterion and construction of Nyquist plot, Bode plot, determination of frequency domain specifications and stability analysis using Nyquist plot and Bode plot.

Unit V: State Variable Analysis [08 Hours]

State space model representation of LTI systems using physical, phase and canonical variables, Relationship between state variable model and transfer function, state transition matrix and its computation by Laplace transform method only, Solution of state equations. Controllability and Observability.

Textbooks:

1. N. J. Nagrath and M. Gopal, "Control System Engineering", New Age International Publishers, 5th Edition.
2. K. Ogata, "Modern Control Engineering", Prentice Hall India Learning Private Limited; 5th Edition.

Reference Books:

1. Benjamin C. Kuo, "Automatic control systems", Prentice Hall of India, 7th Edition.
2. M. Gopal, "Control System – Principles and Design", Tata McGraw Hill, 4th Edition.
3. Schaum's Outline Series, "Feedback and Control Systems" Tata McGraw -Hill.
4. John J. D'Azzo and Constantine H. Houpis, "Linear Control System Analysis and Design", Tata McGraw-Hill, Inc.
5. Richard C. Dorf and Robert H. Bishop, "Modern Control Systems", Addison – Wesley.

Third Year (Semester V)
B. Power Electronics

26AF1378PE509B	Power Electronics	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

The aim of this course is to:

1. To understand the working principles, construction, characteristics, and applications of various power semiconductor devices and their triggering and commutation methods.
2. To study the principles and operation of phase-controlled rectifiers and their performance with different types of loads.
3. To explain the operating principles and control strategies of AC voltage controllers and cycloconverters for various load conditions.
4. To impart knowledge about the working principles, types, and control techniques of inverters and choppers.
5. To introduce the fundamentals of electric drives and their control using different types of power electronic converters.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Identify and compare the characteristics and applications of power semiconductor devices and analyze SCR triggering and commutation circuits.
CO2	Evaluate the performance of single-phase controlled rectifiers and calculate output parameters for different load conditions.
CO3	Analyze the operation of single-phase AC voltage controllers and cycloconverters for R and R-L loads.
CO4	Design and analyze inverter and chopper circuits for single-phase and three-phase applications.
CO5	Apply appropriate converter configurations to control the speed and torque of single-phase electric drives.

Course Contents:

Unit I: Power Semiconductor Devices: [09 Hours]

Principle of operation, construction, characteristics, ratings and applications of: Power Diodes, Power BJT, Power MOSFET, SCR, IGBT, DIAC, TRIAC and GTO. Triggering circuits(R, R-C, and UJT) and Commutation circuits for SCRs.

Unit II: Power Converters: [08 Hours]

Principle of phase control, single phase half wave controlled rectifier, half controlled bridge & fully controlled bridge rectifier for resistive and RL load, derivation for output voltage and current, effect of freewheeling diode, single phase dual converters.

Unit III: A.C. Voltage controllers: [08 Hours]

Integral cycle and phase angle control, single phase A.C. Voltage controller with R, R-L loads. Cyclo-converter Single phase Step-Up Cyclo-converters and Step down cyclo-converters.

Unit IV: Inverters and Chopper **[08 Hours]**

Inverters: Single phase series and parallel inverters, l-Φ bridge Inverter, 3-Φ inverters: 180 mode and 120 mode operation.

Chopper: Basic chopper operation, Four quadrant chopper, voltage commutated and current commutated chopper.

Unit V: Electrical Drives: **[07 Hours]**

Concept of Electric drives, Single phase electrical drives: Half wave converter drives, Semi converter drives, Full converter drives, Dual converter drives.

Textbooks:

1. P.S. Bhimra, "Power electronics", Khanna Publication.
2. M. D. Singh, K. B. Khanchandani, "Power Electronics", Tata McGraw-Hill.
3. Muhammad H. Rashid, "Power electronics" Prentice Hall of India

Reference Books:

1. Ned Mohan, Robbins, "Power electronics", edition III, John Wiley and sons.

Third Year (Semester V)
C. Information Theory & Coding Techniques

26AF1378PE509C	Information Theory & Coding Techniques	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is:

1. To introduce fundamental concepts of information theory including entropy and information measures.
2. To develop understanding of source coding techniques and data compression methods.
3. To explain communication channel models and evaluate channel capacity.
4. To provide knowledge of error detection and correction using block and cyclic codes.
5. To enable understanding of convolutional coding and decoding techniques for reliable communication

Course Outcomes:

On completion of the course, students will be able to:

CO1	Explain information theory concepts such as entropy, information content, and statistical models of sources.
CO2	Apply source coding techniques like Shannon, Shannon-Fano, and Huffman coding for efficient data representation.
CO3	Analyze communication channels and compute mutual information and channel capacity.
CO4	Apply error control coding techniques using linear block codes, Hamming codes, and cyclic codes.
CO5	Explain convolutional encoding and decoding techniques using trellis representation and Viterbi algorithm.

Course Contents:

Unit 01: Information Theory **[7 hours]**

Introduction to information theory, measure of information and information content, average information content of symbols in long independent sequences and dependent sequences, Markov statistical model for information sources, entropy and information rate of Markov sources.

Unit 2: Source Coding **[8 hours]**

Encoding of source output, Shannon's encoding algorithm, Shannon-Fano encoding algorithm, source coding theorem, prefix codes, Kraft–McMillan inequality, Huffman coding.

Unit 3: Information Channels **[9 hours]**

Communication channels, discrete communication channels, channel matrix, joint probability matrix, Binary Symmetric Channel (BSC), system entropies, mutual information, channel capacity, channel capacity of BSC, Binary Erasure Channel (BEC), Muroga's theorem.

Unit 4: Error Control Coding **[8 hours]**

Introduction to error control coding, methods of controlling errors, types of errors and codes, linear block codes including matrix description, error detection and correction, single error correction Hamming code, standard array decoding, cyclic codes including algebraic structure, encoding using shift register, syndrome calculation, error detection and correction.

Unit 5: Convolutional Codes **[8 hours]**

Convolution encoder, time domain approach, transform domain approach, code tree, trellis and state diagram, Viterbi decoding algorithm.

Textbooks:

1. K. Sam Shanmugam, "Digital and Analog Communication Systems", Wiley India Pvt. Ltd., 1996.
2. Simon Haykin, "Digital Communication", Wiley India Pvt. Ltd., 2008.

Reference Books:

1. Ranjan Bose, "Information Theory, Coding and Cryptography", Tata McGraw Hill, 2nd Edition, 2007.
2. J. Das, S. K. Mullick, P. K. Chatterjee, "Principles of Digital Communication", Wiley, 1986.
3. Bernard Sklar, "Digital Communications: Fundamentals and Applications", Pearson, 2nd Edition, 2016.
4. Hari Bhat, Ganesh Rao, "Information Theory and Coding", Cengage, 2017.
5. Todd K. Moon, "Error Correction Coding", Wiley, 2006.

Third Year (Semester VI)
SystemVerilog for Design and Verification

26AF1378PC601	SystemVerilog for Design and Verification	PCC	3L- 0T - 0P	3 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 0 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

The aim of this course is to:

1. Introduce the foundational guidelines of modern hardware verification methodologies, layered testbenches, and advanced System Verilog data types.
2. Develop the ability to write procedural routines, implement System Verilog assertions, and use interface constructs to effectively connect the testbench to the design under test.
3. Impart the core principles of Object-Oriented Programming (OOP) to help students build reusable, modular, and scalable verification environments.
4. Equip students with the concepts and techniques of constrained-random stimulus generation to efficiently explore and test the state space of complex digital designs.
5. Demonstrate the use of interprocess communication mechanisms (events, semaphores, mailboxes) and functional coverage strategies to measure and analyze verification completeness.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Understand the concepts of verification methodologies and data types.
CO2	Summarize the concepts of procedural statements, routines and assertions.
CO3	Illustrate the concepts of OOP terminology.
CO4	Demonstrate the randomization in System Verilog.
CO5	Analyze the concepts of functional coverage.

Course Contents:

UNIT-I: Verification guidelines and Data types [08 Hours]

Verification guidelines: Verification Process, Basic Test bench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Test bench components, Layered test bench, Building layered test bench, Simulation environment phases, Maximum code reuse, Test bench performance.

Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative Arrays, Linked lists, Array methods, choosing a storage type, creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constants, strings, expression width.

UNIT-II: Routines and Connecting the test bench & design [08 Hours]

Procedural statements and routines: Procedural statements, tasks, functions and void Functions, Routine arguments, returning from routine, local data storage, Time values.

Connecting the test bench and design: Separating the test bench and design, Interface constructs, Stimulus timing, Interface driving and sampling, connecting it all together, Top-level scope, Program – Module interactions, System Verilog assertions.

UNIT-III: Basic OOP **[08 Hours]**

Introduction, first class, define a class, OOP (Object Oriented Programming) terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. private, Straying off course, building a test bench.

UNIT-IV: Randomization **[08 Hours]**

Introduction, randomization, Randomization in System Verilog, Constraint details, solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post randomize functions, Constraints tips and techniques, common randomization problems.

UNIT-V: Interprocess communication and Functional Coverage **[08 Hours]**

Interprocess Communication, Events, Semaphores, Mailboxes, Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of a Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, Measuring Coverage Statistics During Simulation.

TEXT BOOKS:

1. Chris Spears, System Verilog for Verification, 2nd Edition, Springer, 2008.

REFERENCES:

1. Vijayaraghavan, Srikanth, and Meyyappan Ramanathan. A practical guide for SystemVerilog assertions , Springer Science & Business Media, 2006.
2. Bergeron, Janick. Writing testbenches using SystemVerilog , 1st Edition,Springer Science & Business Media, 2007.

Third Year (Semester VI)
SystemVerilog for Design and Verification Lab

26AF1378PC602L	**SystemVerilog for Design and Verification Lab**	**PCC Lab**	**0L- 0T - 2P**	**1 Credits**

Teaching Scheme	Examination Scheme
Practical: 02 hrs./week	Continuous Assessment: 60 Marks End Semester Exam: 40 Marks

SystemVerilog for Design and Verification Lab

Minimum 8-10 experiments are to be performed based on contents from syllabus.

Third Year (Semester VI)
Embedded System Design

26AF1378PC603	Embedded System Design	PCC	3L- 0T - 0P	3 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 0 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

The aim of this course is to:

1. Understand the fundamentals, architecture, and design methodology of embedded systems.
2. Develop embedded firmware using Embedded C for ARM Cortex-M based microcontrollers.
3. Understand the architecture and programming features of STM32 microcontrollers.
4. Interface various sensors, actuators, and peripheral devices with STM32 microcontrollers.
5. Apply RTOS concepts to design and implement basic real-time embedded applications.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Understand the fundamentals, architecture, design process, and applications of embedded systems.
CO2	Explore embedded firmware using Embedded C by applying suitable firmware design approaches.
CO3	Illustrate RTOS concepts such as task scheduling and inter-task communication to develop basic real-time embedded system applications.
CO4	Describe the architecture and functional features of STM32 (ARM Cortex-M4) microcontrollers and configure its core peripherals.
CO5	Implement embedded applications by interfacing GPIO, timers, UART, ADC, DAC/PWM, LCD, sensors, and relay modules with STM32 microcontrollers.

Course Contents:

Unit 1: Introduction to Embedded Systems [08 Hours]

Definition of Embedded System, Embedded Systems Vs General Purpose Computing Systems, Characteristics of embedded computing applications, Design Challenge, processor Technology, IC Technology, Classification of Embedded System, Major Application Areas. The embedded system design process-requirements, specification, architecture design, designing hardware and software, components, system integration.

UNIT 2: EMBEDDED FIRMWARE DESIGN AND DEVELOPMENT [08 Hours]

Embedded firmware design approaches-super loop-based approach, operating system-based approach; Embedded firmware development languages-assembly language-based development, high level language-based development; Programming in embedded c.

UNIT 3: - RTOS BASED EMBEDDED SYSTEM DESIGN [08 Hours]

Operating system basics, types of operating systems, tasks, process and threads, multiprocessing and multitasking, task scheduling: non-preemptive and pre-emptive scheduling; task communication-shared memory, message passing.

Unit 4: STM32 Architecture [08 Hours]

STM32 MCU family, ARM architecture, Difference between STM32F1, F4, L series, STM32F407: - Features, Functional Overview: - ARM Cortex-M with FPU core, Memory & Bus Architecture, Power Controller, Reset & Clock control, Direct Memory Access (DMA) controller, Interrupts, Timers and Watchdogs. ARM Thumb. Language support (Assembly, C, C++ and Micro Python).

Unit 5: Programming and Interfacing Applications with STM32 [08 Hours]

Programming: - GPIO, Serial monitor, generate time delay using timer.

Interfacing with STM32 and its programming: - LCD Interfacing, transfer and receive data from PC, read analog voltage and display on serial port, signal generator using DAC, IR sensor interfacing, control AC device using relay module with STM32.

Textbooks:

1. Computers as Components – Wayne Wolf, Morgan Kaufmann (second edition).
2. Introduction to Embedded Systems - Shibu K V, Mc Graw Hill Education.
3. Andrew Sloss, Dominic Symes, Chris Wright, ARM System Developer‘s Guide Designing and Optimizing System Software‖, ELSEVIER.
4. C. Noviello, Mastering STM32: A step-by-step guide to the most complete ARM Cortex-M platform, using a free and powerful development environment based on Eclipse and GCC, 2nd ed. Leanpub, 2022.

Reference Books:

1. Embedded System Design -frank vahid, tony grivargis, john Wiley.
2. Embedded Systems- An integrated approach - Lyla b das, Pearson education 2012.
3. Embedded Systems – Raj Kamal, TMH.
4. An embedded Software Primer, David e Simon, Pearson education.

Third Year (Semester VI)
Embedded System Design Lab

26AF1378PC604L	Embedded System Design Lab	PCC Lab	0L- 0T - 2P	1 Credits

Teaching Scheme	Examination Scheme
Practical: 02 hrs./week	Continuous Assessment: 60 Marks End Semester Exam: 40 Marks

Embedded System Design Lab

(Minimum 8-10 experiments are to be performed based on contents from syllabus)

Sample List of Practical's:

1. Introduction to STM32CubeIDE and STM32CubeMX
2. GPIO Programming – LED Blinking
3. Push Button Interface
4. UART Communication with PC
5. Timer-Based Delay Generation
6. External Interrupt Programming
7. LCD Interfacing
8. ADC Interfacing
9. DAC Signal Generation
10. IR Sensor Interfacing
11. Relay Module Interfacing
12. PWM-Based Servo Motor Control
13. Mini project.

Third Year (Semester VI)
A. Introduction to VLSI Life Cycle & Microfabrication

26AF1378PE605A	Introduction to VLSI Life Cycle & Microfabrication	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Pre-requisite: Basics of CMOS VLSI Design & Digital Logic Design

Course Objectives:

The aim of this course is to:

1. To understand VLSI fundamentals: Gain a solid grasp of VLSI technology, semiconductor materials, and the basics of transistor operation.
2. To Learn about the various stages of the VLSI design lifecycle, including specification, design, verification, synthesis, layout, and fabrication
3. To Explore design methodologies: Introduce different VLSI design methodologies.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Define system specifications, analyse performance and cost metrics, and effectively categorize functional blocks within a complex VLSI design.
CO2	Apply behavioral description using HDLs, perform logic minimization, and understand the process of logic synthesis and functional verification for digital designs.
CO3	Apply circuit optimization techniques and comprehend the steps of physical design including placement, routing, LVS verification, and Design for Manufacturability.
CO4	Perform post-layout simulations, understand PVT variations, utilize PDKs for design verification, and comprehend the purpose of DRC and GDSII for tape-out.
CO5	Describe the fundamental steps of the CMOS fabrication process and explain various integrated circuit packaging techniques.

Course Contents:

Unit 1: **09 Hours**

System & Architectural Design: Defining a system specification, performance analysis, cost analysis, identifying various functional blocks/modules; categorizing them in terms of digital, analog, RF and mixed signal blocks.

Unit 2: **09 Hours**

Functional verification, logic design: Verifying the functionality of blocks, behavioural description, logic minimization, synthesis, verification and testing.

Unit 3: **09 Hours**

Circuit Optimization and Physical Design: Optimization of synthesized blocks for various performance metric, Introduction to placement and route, Layout Vs Schematic (LVS), verification, Design for Manufacturability

Unit 4: **09 Hours**

Tape Out: Post layout simulations, Process Voltage Testing, Process Design Kit, Design Rule Check, GDSII Metalorganic CVD (MOCVD), Plasma Enhanced CVD.

Unit 5: **09 Hours**

Fabrication and Packaging: CMOS process flow, dicing, various types of packaging.

Text Books

1. Sneh Saurabh, "Introduction to VLSI Design flow", Cambridge University Press.
2. N. H. E. Weste and C. Harris, "Principles of CMOS VLSI Design: A System Perspective, 3rd Edition, Pearson Education 2007.

Reference Books

1. M. Morris Mano and Michel. D. Ciletti, Digital Design with an introduction to HDL,
2. VHDL and Verilog, Sixth edition Pearson education. K. Lal Kishore – "VLSI Design", Pearson Education / PHI Learning.

Third Year (Semester VI)
B. Digital VLSI Design

26AF1378PE605B	Digital VLSI Design	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

The aim of this course is to:

1. Examine the voltage transfer characteristics and switching performance of advanced pass-transistor and differential logic families.
2. Analyze the operational phases and signal integrity vulnerabilities inherent in dynamic CMOS circuits.
3. Illustrate the architectural configurations and critical timing constraints of synchronous sequential logic registers.
4. Outline the hierarchical memory architectures and the structural design of static and dynamic memory core cells.
5. Apply fundamental dataflow, behavioral, and structural modeling styles in VHDL to describe digital hardware.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Compare the transistor count, power dissipation, and logical efficiencies of pseudo-NMOS and complementary pass-transistor networks.
CO2	Evaluate charge sharing, leakage, and inversion issues within precharge-evaluate domino logic cascades.
CO3	Calculate setup times, hold times, and maximum operating frequencies for edge-triggered and pulse-based sequential circuits.
CO4	Develop basic hardware descriptions and simulation testbenches for primitive digital components using VHDL.
CO5	Differentiate between the read/write circuitry and timing parameters of ROM, SRAM, and DRAM semiconductor arrays.

COURSE CONTENTS:

UNIT-I: ADVANCED COMBINATIONAL LOGIC FAMILIES [08 Hours]

Ratioed Logic: Pseudo-NMOS logic, voltage transfer characteristics, asymmetric rise/fall times, and static power dissipation calculations, Transistor Equivalency.

Advanced Pass-Transistor Logic: Complementary Pass-transistor Logic (CPL), NAND & NOR gate using CPL, CPL full adder, and layout considerations for pass-gate networks.

Differential CMOS Circuits: Differential CMOS Circuits principles, Examples of Differential CMOS Circuits realizations of and /or functions, complex logic function.

UNIT II: DYNAMIC CMOS CIRCUITS [09 Hours]

Clocked CMOS logic: Principal of Operation, its advantage & drawback, Design of Shift Register, D latch design, D flip flop using Clocked CMOS logic.

Precharge / Evaluate Dynamic CMOS Logic: Principal of Operation, its advantage & drawback, charge sharing, Cascading Problem in Dynamic CMOS logic, Realization of complex logic function in PE logic.

Domino CMOS logic: Principal of Operation, its advantage & drawback, Domino logic with weak pull-up, cascaded domino logic, comparison of domino logic vs static CMOS logic, Inversion issue in Domino logic, Realization of complex logic function in domino logic, Charge Sharing and Charge leakage problems, NORA logic, Zipper CMOS circuits.

UNIT III: SEQUENTIAL LOGIC DESIGN AND TIMING CONSTRAINTS [08 hours]

Latches and Flip-Flops: Latches vs Flipflops or registers**,** Bistability Principle, multiplexer-based latches, and Master-Slave edge-triggered Register.

Advanced Sequential Circuits: Dynamic transmission-gate registers and True Single-Phase Clocking (TSPC) registers, Alternate Register Styles: Pulse Registers, Sense-Amplifier Based Registers, Pipelining: An approach to optimize sequential circuits, Non-Bistable Sequential Circuits: The Schmitt Trigger

Timing Analysis: Setup time, hold time, clock-to-Q delay calculations, and determining the maximum clock frequency. Synchronous design concepts, clock skew, and clock jitter.

UNIT IV: SEMICONDUCTOR MEMORIES [08 Hours]

Introduction: Memory, Memory classification, Classification of Memory: size, foreground vs background memory, Static vs Dynamic Memory, Timing Parameters, Memory classification based on function, Access pattern, Memory Architectures and Building Blocks, Memory Core, Read-Only Memory (ROM) Circuits, Static Read-Write Memory (SRAM) Circuits, Dynamic Read-Write Memory (DRAM) Circuits.

UNIT V: INTRODUCTION TO VHDL [08 Hours]

VHDL Fundamentals, basic anatomy of VHDL code, Basic Data Types & Signals, Three Modeling Styles: Dataflow Modeling, Behavioral Modeling, Structural Modeling, Simulation & Verification.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici "CMOS Digital Integrated Circuits Analysis and Design", TMH, 3rd Ed., 2011.
2. John P. Uyemura, "CMOS LOGIC CIRCUIT DESIGN", KLUWER ACADEMIC PUBLISHERS, 2002
3. Ken Martin, "Digital Integrated Circuit Design", Oxford Press, 2000.
4. Neil H.E. Weste and Harris ,"CMOS VLSI Design: A Circuits and Systems Perspective".
5. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd Ed., PHI.

REFERENCES:

1. Neil H.E. weste and Kamran Eshraghian , "Principles of CMOS VLSI design: A system Perspective".
2. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press, 2011
3. John Wakerly, "Digital Design – Principles and Practices", Pearson.

Third Year (Semester VI)
C. Computer Networks

26AF1378PE605C	Computer Networks	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is:

1. To introduce students to the fundamental concepts of computer networks and layered architectures (OSI & TCP/IP models).
2. To explain the principles, issues, and protocols at the data link layer.
3. To provide insight into routing algorithms, internetworking, addressing and congestion control at the network layer.
4. To help students understand transport layer protocols and connection management techniques.
5. To explore various application layer protocols and real-world services such as DNS, email, and web applications.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Describe the basic structure and functioning of computer networks and reference models (OSI & TCP/IP).
CO2	Explain error detection, correction methods, and different protocols used in data communication.
CO3	Analyze routing techniques, congestion control algorithms, addressing and quality of service mechanisms.
CO4	Compare and evaluate the features of transport layer protocols, especially TCP and UDP.
CO5	Demonstrate understanding of application layer protocols like DNS, HTTP, SNMP, and email systems.

COURSE CONTENTS:

Unit I: INTRODUCTION **[08 Hours]**

Network hardware, Network Software, Network Topologies, Modes of Communication: Simplex, Half Duplex, Full Duplex, Types of networks: LAN, MAN, WAN, OSI Reference Model, TCP/IP Reference models, Internet.

Physical Layer: Guided Transmission media: twisted pairs, coaxial cable, fiber optics, Wireless transmission.

Unit II: THE DATA LINK LAYER **[08 Hours]**

ARQ Protocols: Automatic Repeat Request (ARQ), Stop-and-Wait ARQ, Go-Back-N ARQ, Selective Repeat ARQ, Sliding window protocols. **HDLC:** Configurations and Transfer Modes.
Random Access Protocols: ALOHA, Slotted ALOHA, CSMA, CSMA/CD, CSMA/CA.
Controlled Access Protocols: Reservation, Polling, Token Passing, TDMA, FDMA, CDMA.
Ethernet: Ethernet Standards (IEEE 802.3), Ethernet Frame Format, Wireless LAN: Architecture.

Unit III: THE NETWORK LAYER [08 Hours]

Design issues, Routing algorithms: shortest path routing, Flooding, Hierarchical routing, Broadcast, Multicast, distance vector routing, Congestion Control Algorithms, IPv4 addressing and IPv6 addressing, comparison of IPv4 and IPv6, Quality of Service, Internetworking.

Unit IV: THE TRANSPORT LAYER [08 Hours]

Transport Services, Client/Server Paradigm, Connectionless Versus Connection-Oriented Service, Connection management, TCP and UDP protocols: Header (Segment) format, Connection Establishment, Handshaking, Data transfer, Connection Termination.

Unit V: THE APPLICATION LAYER [08 Hours]

Application Layer –Domain name system, SNMP, Electronic Mail; the World WEB, HTTP, Streaming audio and video.

Textbooks:

1. A. S. Tanenbaum (2003), Computer Networks, 4th edition, Pearson Education/ PHI, New Delhi, India.
2. 1. Behrouz A. Forouzan (2006), Data communication and Networking, 4th Edition, Mc Graw-Hill, India.
3. Achyut S Godbole, "Data Communication and Networking", Tata McGraw-Hill, 1st Edition.

Reference Books:

1. Kurose, Ross (2010), Computer Networking: A top-down approach, Pearson Education, India.
2. Wayne Tomasi, "Introduction to Data Communication and Networking", Pearson Education, 1st Edition.
3. Greg Tomsho, Ed Tittel, David Johnson. "Guide to Networking Essentials", Thomson India Learning, 5th Edition, 2007.
4. William Stallings, "Data and Computer Communication", Pearson Education, 8th Edition, 2000

Third Year (Semester VI)
A. IC Packaging

26AF1378PE607A	IC Packaging	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

The aim of this course is to:

1. Understand the fundamentals, evolution, and importance of IC packaging technologies.
2. Explain semiconductor packaging materials and various interconnection techniques used in IC packaging.
3. Apply thermal management principles and analyze signal and power integrity issues in packaged ICs.
4. Compare different IC packaging types and evaluate their trade-offs for various applications.
5. Understand reliability, testing methods, and recent advancements in semiconductor packaging technologies.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Explain the fundamentals, evolution, and types of IC packaging technologies.
CO2	Describe semiconductor packaging materials and interconnection techniques used in IC packaging.
CO3	Apply thermal management concepts to improve the performance and reliability of IC packages.
CO4	Compare different IC packaging types and select suitable packaging based on application requirements.
CO5	Explain IC package reliability, testing techniques, and recent trends in advanced packaging technologies.

Course Contents:

Unit 1: Introduction to IC Packaging Technologies [08 Hours]

Overview of IC packaging and its significance. Historical context and evolution of packaging technologies. Introduction to packaging types: through-hole, surface-mount, ball grid array.

Unit 2: Packaging Materials and Interconnection Techniques [08 Hours]

Study of materials used in semiconductor packaging. Interconnection techniques: wire bonding, flip-chip, and solder bump technologies.

Unit 3: Thermal Management in IC Packaging [08 Hours]

Principles of thermal management in IC packaging. Techniques for heat dissipation and cooling, Signal integrity challenges in IC packaging, Power integrity considerations and solutions.

UNIT 4: Packaging Types and Trade-offs [08 Hours]

In-depth study of through-hole, surface-mount, and ball grid array packaging, Trade-offs involved in selecting packaging types.

Unit 5: Reliability in IC Packaging **[08 Hours]**

Factors affecting reliability in IC packaging, Testing and validation techniques for packaged ICs, Advanced Topics in IC Packaging, Emerging trends in IC packaging technologies, Advanced materials and techniques.

TEXT BOOKS

1. John H. Lau. Semiconductor Advanced Packaging. Springer, 2021.
2. King-Ning Tu, Chih Chen, Hung-Ming Chen. Electronic Packaging Science and Technology. John Wiley and Sons Inc., 2022.
3. John H. Lau, Flip Chip Technologies
4. John H. Lau, Chip on Board
5. Ball Grid Array Technology Author: John H. Lau

REFERENCE BOOKS

1. William CraigSergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits‖, Tata McGraw Hill, Integrated Circuit Packaging, Assembly and Interconnections
2. Andrea Chen Randy Hsiao-Yu Lo, Semiconductor Packaging
3. Charles A. Harper, Electronic Packaging and Interconnection Handbook
4. Rao R. Tummala - Madhavan Swaminathan, System-on Package (SOP)

Third Year (Semester VI)
B. Electromagnetic Field Theory

26AF1378PE607B	Electromagnetic Field Theory	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. To understand fundamentals of orthogonal coordinate systems and interrelation with 1-D, 2-D & 3-D vectors.
2. To impart knowledge of Static Electric field, Static Magnetic field and the associated laws with various boundary conditions for static and time varying electric and magnetic fields.
3. To analyze and understand the concepts of propagation of EM waves.
4. To understand, analyze and evaluate the radiation of electromagnetic wave.

Course Outcomes: On completion of the course, students will be able to:

CO1	Apply vector calculus for solution to electric and magnetic field problems.
CO2	Analyze the concepts of Electrostatic fields.
CO3	Analyze the concepts of static magnetic fields.
CO4	Describe Boundary conditions in electromagnetic and Maxwell's equations.
CO5	Describe the electromagnetic wave and its propagation in different homogeneous media.

Course Contents:

UNIT – 1 Review of Vector Analysis **08 Hours**

Cartesian, Cylindrical and Spherical Co-ordinate Systems, Vector products, Projection of Vectors, Gradient, Divergence and Curl, line, surface & volume integrals, Divergence theorem and Stokes theorem.

UNIT – 2 Electrostatics **08 Hours**

Coulomb's Law, Electric field intensity, Evaluation of Electric field intensity due to line charge, Surface charge and Volume charge distribution, Electric flux and Electric flux density, Gauss Law, Electrostatic potential, Potential gradient, Electric dipole and Polarization.

UNIT – 3 Magnetostatics **08 Hours**

Biot–Savart Law, Ampere's Circuital Law, Magnetic field intensity, Magnetic field intensity evaluation due to infinite, finite and circular current carrying conductors, Magnetic flux and Flux density, Magnetic dipole and Magnetization.

UNIT – 4 Boundary Conditions & Maxwell's Equations **08 Hours**

Boundary condition at Dielectric – Conductor interface, Dielectric – Dielectric interface, Boundary conditions for magnetic materials interface, Current continuity equation, Maxwell's equations.

UNIT – 5 Electromagnetic wave propagation and application 08 Hours

Electromagnetic wave equation for free space, lossy dielectric material and perfect conductor, Propagation constant, Attenuation constant & Phase shift constant, Skin depth, Poynting Theorem, Reflection of a plain wave in a normal incidence at Dielectric – Dielectric interface. Applications of EM Waves: Electromagnetic Compatibility (EMC), Microwave-ovens, Antenna, wireless communication systems.

TEXT BOOKS:

1. Hayt W.H.: "Engineering Electromagnetic" Tata Mc Grawhill E.C. Jordan & K.G. Balmain, Electromagnetic waves & Radiating Systems, Prentice Hall, India
2. Jordan E.C. and Balamin K.C.: "Electromagnetic Waves and Radiating System "Prentice Hall of India Private Limited.
3. Krauss, "Electromagnetics", McGraw Hill, New York, 4th edition.

REFERENCE BOOKS:

1. Mathew N.O., Sadiku "Principles of Electromagnetics" (Fourth Edition), Oxford University Press.
2. Ramo S. and Whinnery R.: "Fields and Waves in Communication Electronics" John Wiley and sons, New Delhi.
3. Dr. TVS Arun Murthy, "Electromagnetic Fields (Theory & Problems)" S. Chand & Company Ltd.

Third Year (Semester VI)
C. Advanced Communication Technology

26AF1378PE607C	Advanced Communication Technology	PEC	3L- 1T - 0P	4 Credits

Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Pre-requisite: Basics of Advanced Communication Technology.

Course Objectives: The aim of this course is to:

1. Explain the principles of satellite communication, orbital mechanics, and satellite system components.
2. Describe satellite-based communication services, navigation systems, and GPS technology.
3. Illustrate the operating principles and transmission characteristics of optical fiber communication.
4. Interpret the working of optical sources, detectors, and modern optical communication devices.
5. Summarize the architecture, technologies, and applications of 5G wireless communication.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the concepts of satellite communication, orbital parameters, satellite transponders, and propagation characteristics.
CO2	Describe the architecture and operation of VSAT systems, GPS, and satellite navigation services.
CO3	Illustrate the principles of optical fiber propagation, transmission characteristics, and wavelength division multiplexing.
CO4	Interpret the operating principles of optical sources, semiconductor lasers, LEDs, and optical detectors.
CO5	Summarize the architecture, key technologies, and applications of 5G communication, IoT integration, and Massive MIMO.

Course Contents:

UNIT I: Satellite Communication **[08 Hours]**

Satellite frequency bands, Satellite types-LEO, MEO, GEO, HEO, Uplink, Downlink, Cross link, Kepler's laws, Satellite orbits, Geo-stationary Satellite. Orbital Aspects of Satellite Communication: Orbital period and velocity, Effect of orbital inclination, Azimuth and Elevation, Converge angle and Slant range, Satellite Transponder, Electromagnetic field Propagation, Atmospheric Losses, Receiver noise, Carrier to noise ratio, Frequency reuse and depolarization.

UNIT II: Satellite Services **[08 Hours]**

Very Small Aperture Satellite (VSAT): Overview of VSAT system, Network architecture, VSAT antennas, Transmitter and Receiver. Satellite Navigation and Global Positioning System (GPS): Radio and Satellite navigation, Position, Location in GPS, GPS receivers and codes, GPS navigation message and signal levels, Timing accuracy, GPS receiver operation.

UNIT III: Optical Fiber Waveguide and Transmission Characteristics [08 Hours]

Ray Theory of Optical Fiber, Total internal reflection, Snell's law, Acceptance Angles, Numerical Aperture (NA), Modes in Optical Fiber, Single mode and Multimode Optical Fiber, Power flow. Transmission Characteristics of Optical Fiber: Attenuation, Absorption losses, scattering losses, Bending losses, Dispersion, Intermodal and Intramodal Dispersion; Concept of Wavelength Division Multiplexing.

UNIT IV: Optical Sources and Detectors [08 Hours]

Optical Sources: Optical Emission from Semiconductor, LED, Power, Efficiency, Double heterojunction LED, Basic concept of LASER, Semiconductor injection LASER.

Optical Detectors: Optical detection principle, Absorption, quantum efficiency, Responsivity, PIN Photodiode, Avalanche Photodiode and Phototransistor.

UNIT V: Introduction to 5G Technology [08 Hours]

Historical trend and evolution of LTE technology to beyond 4G – Key building blocks of 5G, Specification requirements for driving 5G technology, 5G Use Cases and System Concepts – The 5G Architecture – IoT in relation to 5G; Massive MIMO: Fundamentals, Advantages.

TEXTBOOKS:

1) Gagliardi Robert M., "Satellite Communication", CBS Publication and Distributers, New Delhi
2) Senior J.M., "Optical Fiber communication and Application", Prentice Hall of India Pvt. Ltd, New Delhi.
3) Wei Xiang, Kan Zheng, Xuemin (Sherman) Shen, - 5G Mobile Communications, Springer, 2017.

REFERENCE BOOKS

1) Gowar, "Optical Communication System", Prentice Hall.
2) R. P. Khare, "Fiber Optics and Opto Electronics", Oxford University Press, First Edition.
3) G. Keiser, "Optical Fiber Communication", McGraw Hill International Book Co. New York.
4) Pratt Timothy and Bostian W. Charles, "Satellite Communication", Willey International Publication, New York.
5) Afif Osseiran, Jose F. Monserrat and Patrick Marsch, - 5G Mobile and Wireless Communications Technology, Cambridge University Press, 2016.

Third Year (Semester VI)
Basic Concepts of Film & Video Editing

26AF1378SE608	Basic Concepts of Film & Video Editing	PEC	1L- 0T - 2P	2 Credits

Teaching Scheme	Examination Scheme
Lecture: 1 hrs./week Practical: 2 hr./week	Continuous Assessment: 60 Marks End Semester Exam: 40 Marks

Course Objectives:

The aim of this course is to:

1. Provide an overview of the history and evolution of film editing, including its invention and significant milestones.
2. Explore the impact of editing on the language of cinema and how it shapes narrative and emotional engagement.
3. Teach the fundamental technical skills required for effective film editing, including the basic joining of shots.
4. Introduce students to advanced concepts in editing, such as complex narrative structures and the psychological effects of editing choices.
5. Enable students to apply these concepts and techniques practically, culminating in the ability to edit their own simple narrative film.

Course Outcomes:

On completion of the course, students will be able to:

CO1	Understand the Historical Context of Film Editing: Articulate the historical development of film editing and its role in the evolution of cinema.
CO2	Recognize the Impact of Editing on Storytelling: Analyze how different editing techniques influence the narrative flow and emotional impact of a film
CO3	Demonstrate Technical Proficiency: Apply technical knowledge to perform basic editing tasks, including cutting and joining shots.
CO4	Construct Complex Narratives: Utilize editing techniques to build and understand complex narrative structures in film.
CO5	Produce a Simple Narrative Film: Independently edit a simple narrative film, showcasing an understanding of both technical skills and creative storytelling.

Course Contents:

Unit 1: **08 Hours**

Basic Concepts of Editing, Creative Role of the Editor.

Unit 2: **08 Hours**

Basic Aspects of Film Editing, Techniques of Joining Two Shots, Match Cut, Invisible Cut etc, Imaginary Line, 30 Degree Rule etc, Methods and techniques.

Unit 3: **08 Hours**

Narrativisation, Digital Editing Software and Equipment, Editing Basics.

Unit 4: **08 Hours**

FCP Introduction, Interface, Capturing and Transferring Video, Basic editing Functions, Image Sizes, Settings and Motion Tab.

Unit 5: **08 Hours**

Manipulations, Audio, Key Framing and Text, Colour Correction & Chroma Keying, Short Cuts and Exports.

Text Books:

1. Walter Murch; “In the blink of an Eye”.
2. Ken Dancyger; “The Technique of Film and Video Editing”.
3. Edward Dmytryk; “On Film Editing”; An introduction to the Art of Film Construction.
4. Sergei Eisenstein; “Film Form”, “Essays in Film Theory and the Film Sense”.
5. Vincent LoBrutto; “Selected Takes”; Film Editors on Editing.

Reference Books:

1. David Mamet; “On Directing Film”.
2. Richard d. Pepperman; “The Eye is Quicker”.
3. Bobbie O’Steen; “The Invisible Cut”.
4. Karel Reisz, Gavin Millar; “The Technique of Film Editing”.
5. Roger Critttenden; “Fine Cuts”.